

● General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

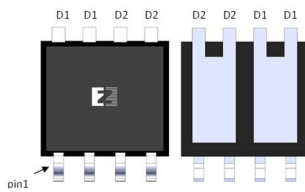
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low thermal resistance
- AEC-Q101 qualified

● Application

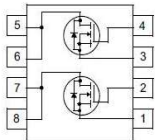
- BLDC motor driver
- DC-DC
- Load switch



● Product Summary



LPAK56D



$V_{DS}=40V$

$R_{DS(ON)}=4.1m\Omega$

$I_D=96A$



● Ordering Information

Part NO.	ZMDA68410HLF
Marking	68410H
Packing information	REEL TAPE
Basic ordering unit (pcs)	3000

● Absolute Maximum Ratings FET1 and FET2 ($T_A=25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}	$25^\circ C \leq T_J \leq 175^\circ C$	-	40	V
Gate-source voltage ^①	V_{GS}	DC; $-55^\circ C \leq T_J \leq 175^\circ C$	-20	20	V
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^\circ C$	-	96	A
	I_D	$V_{GS}=10V, T_C=75^\circ C$	-	78	A
	I_D	$V_{GS}=10V, T_C=100^\circ C$	-	68	A
Pulsed drain current	I_{DM}	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	384	A
Diode continuous current	I_S	$V_{GS}=0V, T_C=25^\circ C$	-	63	A
Diode pulse current	$I_{S,pulse}$	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	252	A
Total power dissipation	P_D	$V_{GS}>6V, T_C=25^\circ C$	-	82	W
Total power dissipation	P_D	$V_{GS}>6V, T_A=25^\circ C$	-	1.7	W
Operating junction temperature	T_J		-55	175	$^\circ C$
Storage temperature	T_{STG}		-55	175	$^\circ C$
Single pulse avalanche energy	E_{AS}	$L=0.1mH, V_{GS}=10V, R_g=25\Omega$,	-	61	mJ

Single pulse avalanche energy	E_{AS}	$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	-	110	mJ
ESD level (HBM)	CLASS 1B				

● Thermal resistance FET1 and FET2

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	1.84	$^{\circ}\text{C/W}$
Thermal resistance, junction - ambient	$R_{thJA}^{(2)}$	-	-	86	$^{\circ}\text{C/W}$
Soldering temperature	T_{sold}	-	-	260	$^{\circ}\text{C}$

● Electronic Characteristics FET1 and FET2 ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

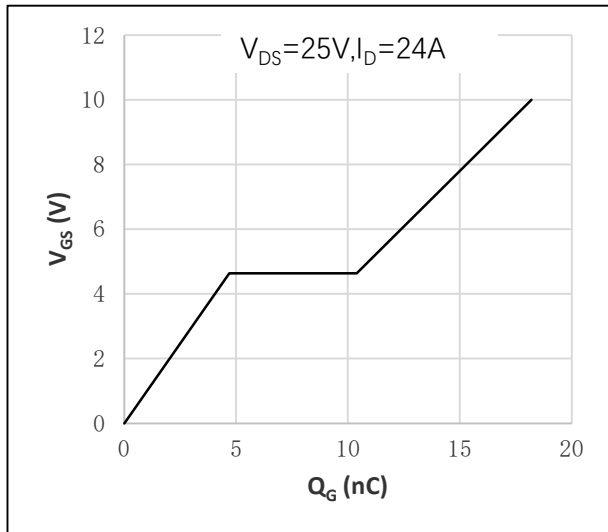
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$	40	-	-	V
		$V_{GS}=0\text{V}$, $I_D=250\mu\text{A}$, $T_j=-55^{\circ}\text{C}$	38	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}$, $I_D=250\mu\text{A}$	2	2.8	4	V
		$V_{GS}=V_{DS}$, $I_D=1\text{mA}$, $T_j=175^{\circ}\text{C}$	1.2	-	-	V
		$V_{GS}=V_{DS}$, $I_D=1\text{mA}$, $T_j=-55^{\circ}\text{C}$	-	-	4.3	V
Drain-source leakage current	I_{DSS}	$V_{GS}=0\text{V}$, $V_{DS}=40\text{V}$	-	-	1	μA
		$V_{GS}=0\text{V}$, $V_{DS}=40\text{V}$, $T_j=175^{\circ}\text{C}$	-	-	500	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20\text{V}$, $V_{DS}=0\text{V}$	-	-	100	nA
Static drain-source on resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=24\text{A}$, $T_j=25^{\circ}\text{C}$	-	4.1	4.9	m Ω
		$V_{GS}=10\text{V}$, $I_D=24\text{A}$, $T_j=175^{\circ}\text{C}$	-	7.4	8.9	m Ω
Forward transconductance	g_{FS}	$V_{DS}=5\text{V}$, $I_{SD}=10\text{A}$	-	12.8	-	S
Diode forward voltage	V_{FSD}	$V_{GS}=0\text{V}$, $I_{SD}=24\text{A}$	-	-	1.3	V

● Dynamic characteristics FET1 and FET2 ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

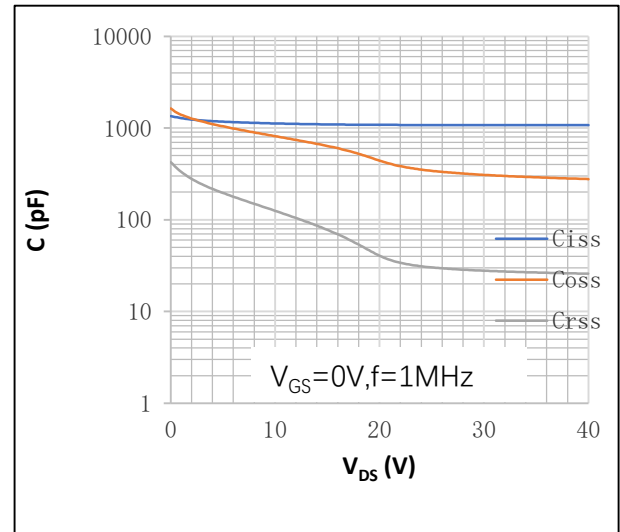
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1\text{MHz}$, $V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$	-	1082	-	pF
Output capacitance	C_{oss}		-	335	-	pF
Reverse transfer capacitance	C_{rss}		-	36	-	pF
Gate resistance	R_g	$f=1\text{MHz}$	-	2.5	-	Ω
Total gate charge	Q_g	$V_{DD}=25\text{V}$, $I_D=24\text{A}$, $V_{GS}=10\text{V}$	-	18.2	-	nC
Gate-source charge	Q_{gs}		-	4.7	-	nC
Gate-drain charge	Q_{gd}		-	5.7	-	nC

Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=32V,$ $R_G=5\Omega, I_D=20A$	-	8	-	ns
Turn-on rise time	t_r		-	5	-	ns
Turn-off delay time	$t_{D(off)}$		-	13	-	ns
Turn-off fall time	t_f		-	8	-	ns
Reverse recovery time	t_{rr}	$V_{DD}=20V, di_s/dt = 100A/us,$ $I_s=20A$	-	21	-	ns
Reverse recovery charge	Q_{rr}		-	481	-	nC

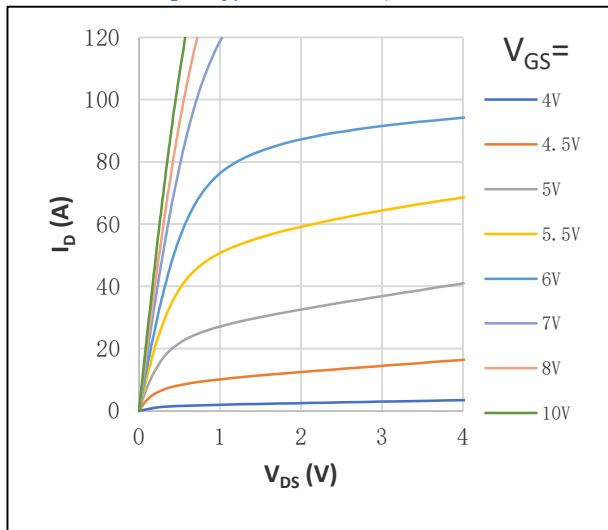
● Fig.1 Gate-source voltage as a function of gate charge; Typical values; $T_j=25^\circ\text{C}$



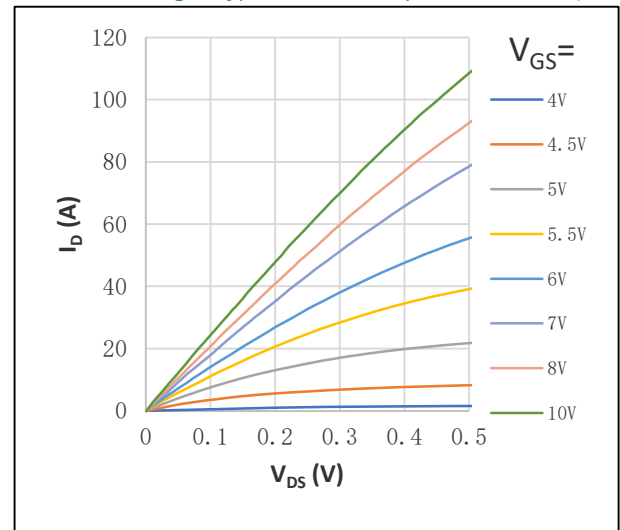
● Fig.2 Input, output and reverse transfer capacitances as a function of drain-source voltage; Typical values; $T_j=25^\circ\text{C}$



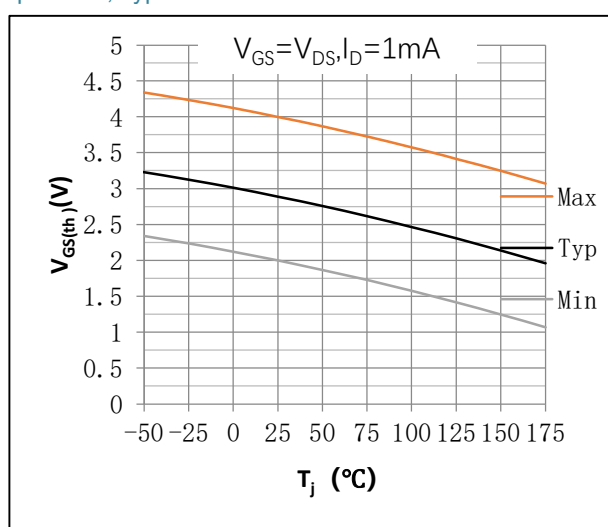
● Fig.3 Output characteristics: drain current as a function of drain-source voltage; Typical values; $T_j=25^\circ\text{C}$



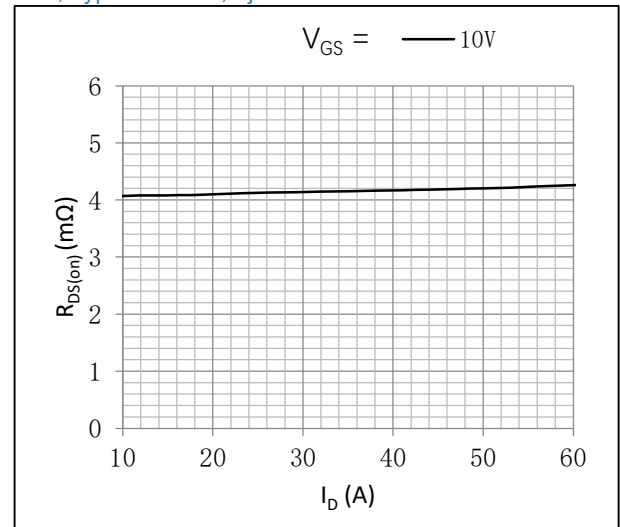
● Fig.4 Output characteristics: drain current as a function of drain-source voltage; Typical values: Expanded curve; $T_j=25^\circ\text{C}$



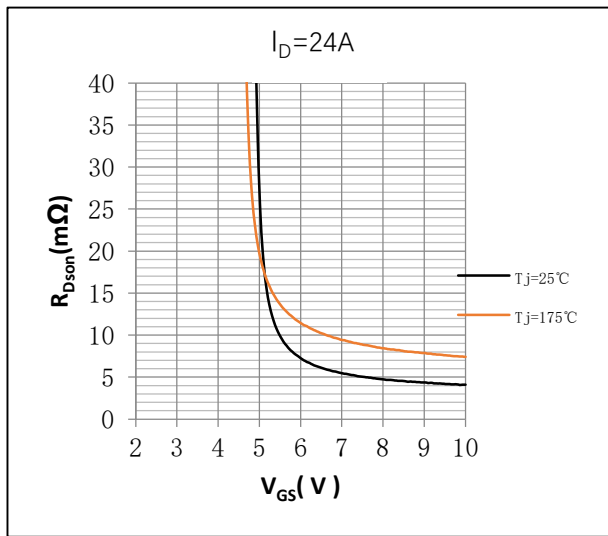
● Fig.5 Gate-source threshold voltage as a function of junction temperature; Typical/min/max values



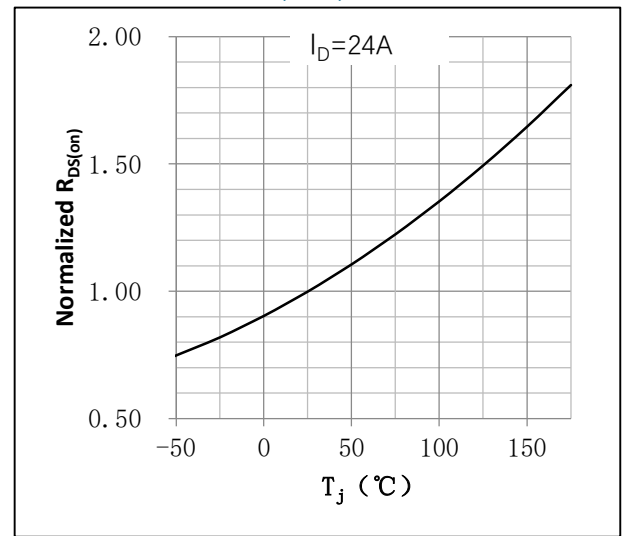
● Fig.6 Drain-source on-state resistance as a function of drain current; Typical values; $T_j=25^\circ\text{C}$



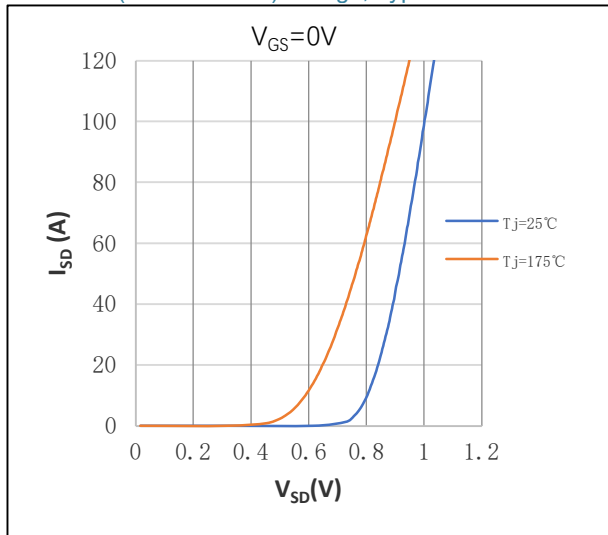
● Fig.7 Drain-source on-state resistance as a function of gate-source voltage; Typical values



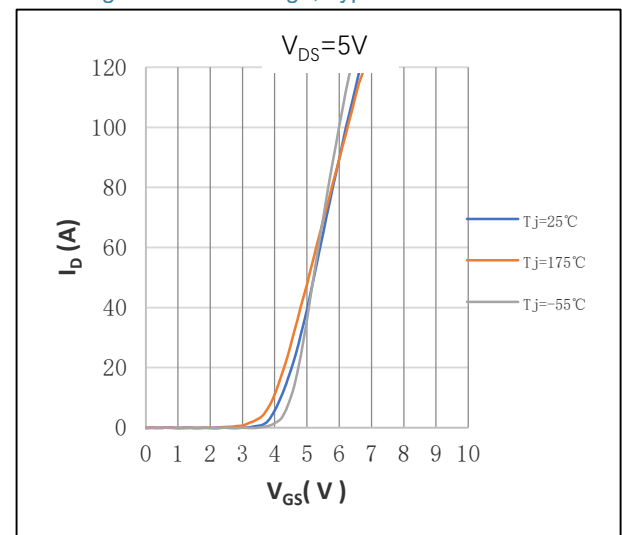
● Fig.8 Normalized drain-source on-state resistance factor as a function of junction temperature; Typical values Normalized On-Resistance= $R_{DS(on)}/R_{DS(on)}(25^\circ C)$



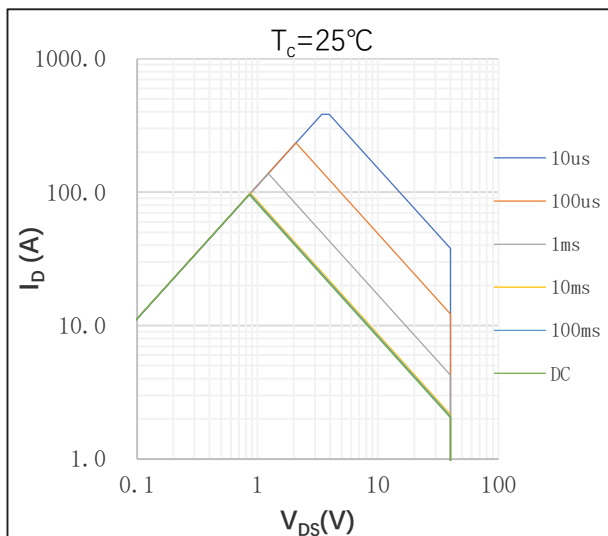
● Figure 9. Source (diode forward) current as a function of source-drain (diode forward) voltage; Typical values



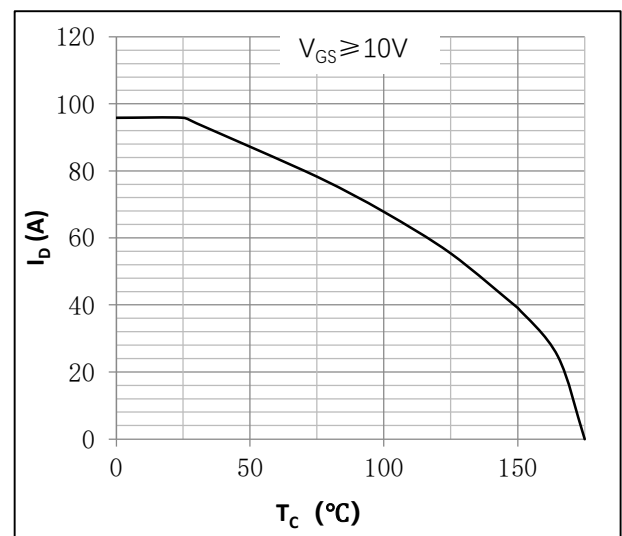
● Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; Typical values



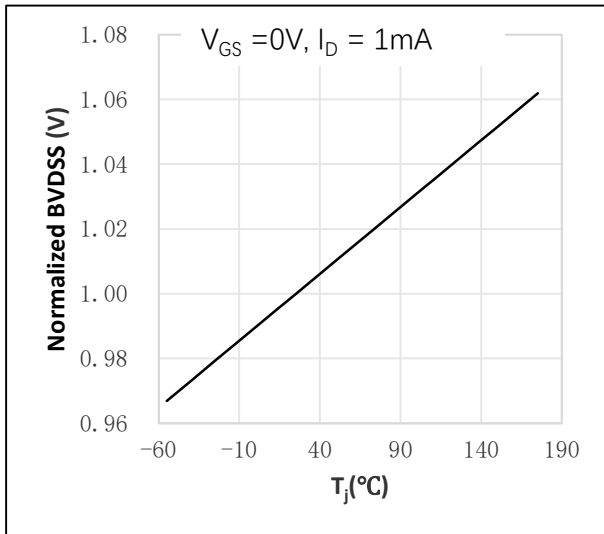
● Fig.11 Safe operating area: continuous and peak drain currents as a function of drain-source voltage; Calculative values



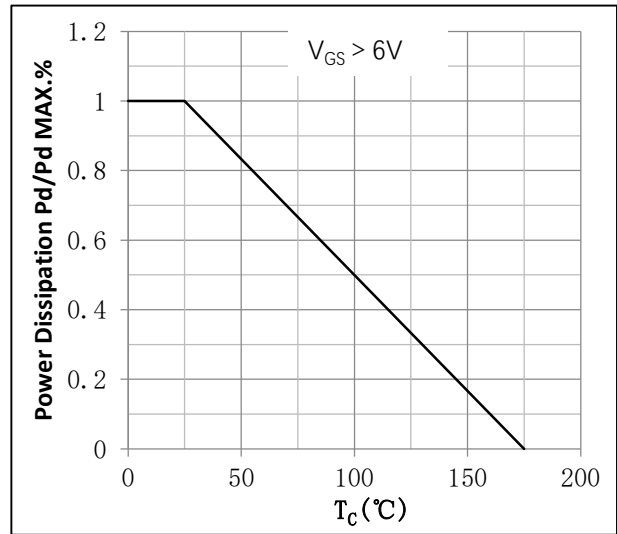
● Fig.12 Continuous drain current as a function of case temperature³; Calculative values



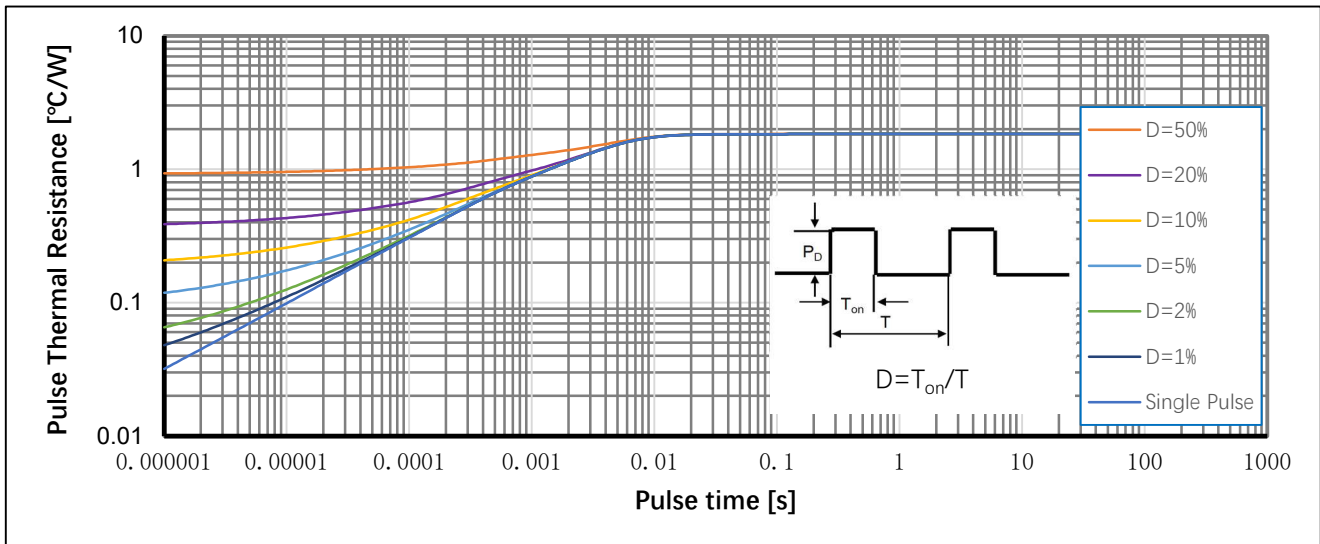
● Fig.13 Drain-source breakdown voltage as a function of junction temperature; Typical values Normalized $BV_{DSS} = BV_{DSS}/BV_{DSS}(25^{\circ}\text{C})$



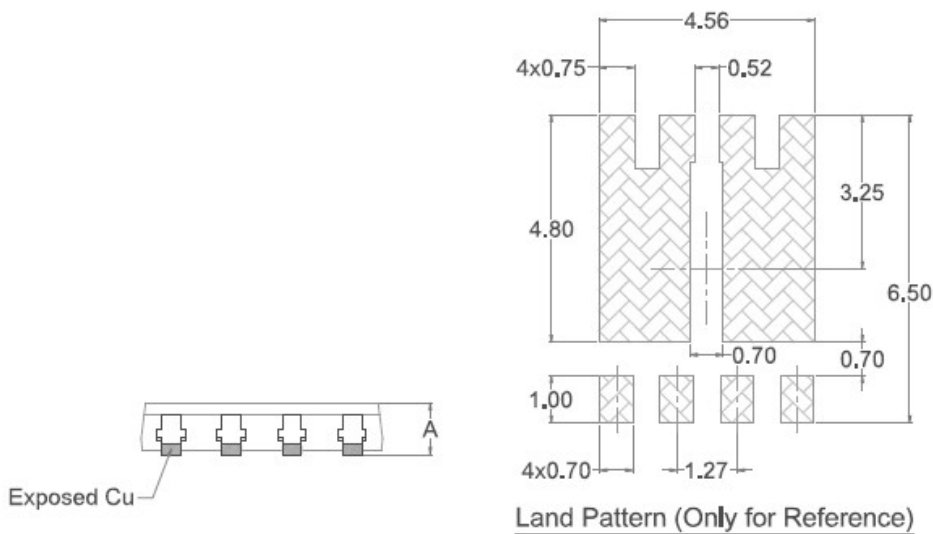
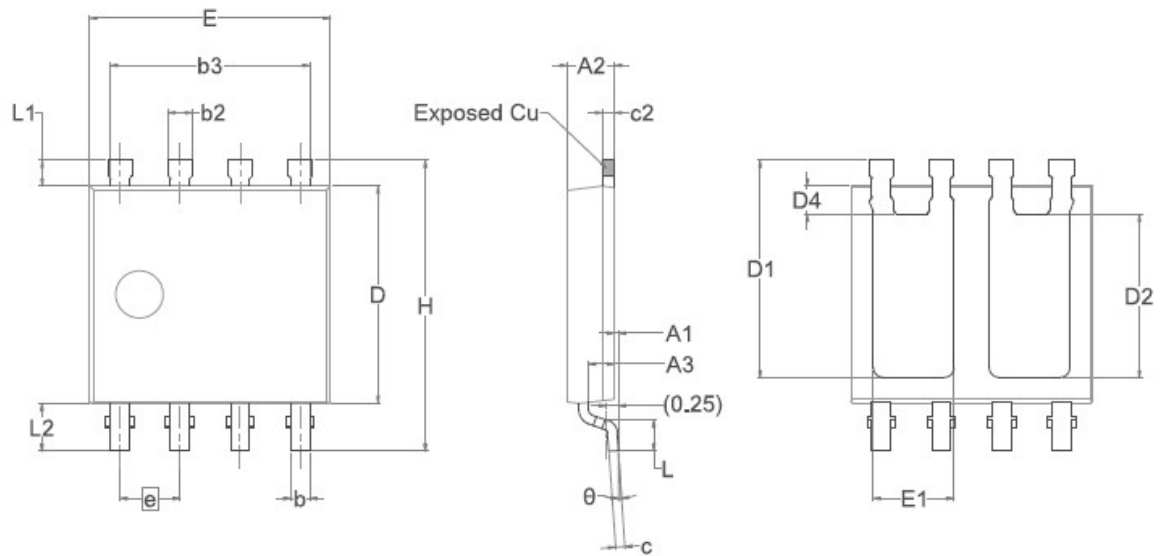
● Fig.14 Normalized total power dissipation as a function of case temperature; Calculative values Normalized Power Dissipation $= P_d/P_d(25^{\circ}\text{C})$



● Fig.15 Transient thermal impedance from junction to case as a function of pulse duration; max values



● Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	1.01	1.10	1.20
A1	0.00	---	0.15
A2	0.95	1.00	1.10
A3	0.50	0.55	0.65
b	0.35	0.40	0.50
b2	0.37	0.52	0.67
b3	4.21 REF.		
c	0.19	0.20	0.25
c2	0.22	0.25	0.28
D	4.45	4.60	4.70
D1	4.60 REF.		
D2	3.25	3.45	3.65
D4	0.45	0.60	0.75
E	4.90	5.10	5.30
E1	1.60	1.70	1.80
e	1.27 BSC.		
H	5.95	6.15	6.35
L	0.45	0.65	0.85
L1	0.40	0.55	0.70
L2	0.80	1.00	1.30
θ	0°	4°	8°

● Note

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on 1 square inch FR-4 substrate PCB, 1oz copper, minimum footprint, tested in a still air environment with $T_A=25^{\circ}C$;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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● Revision History

Version	Date	Change
A	2025/11/7	New
B	2026/4/16	1. Update package name as LFPAK56D 2. Correct marking information. 3. Add Bvdss minimum value 4. Add VTH hot/cold spec. 5. Add diode current rating 6. Add IDSS hot spec.